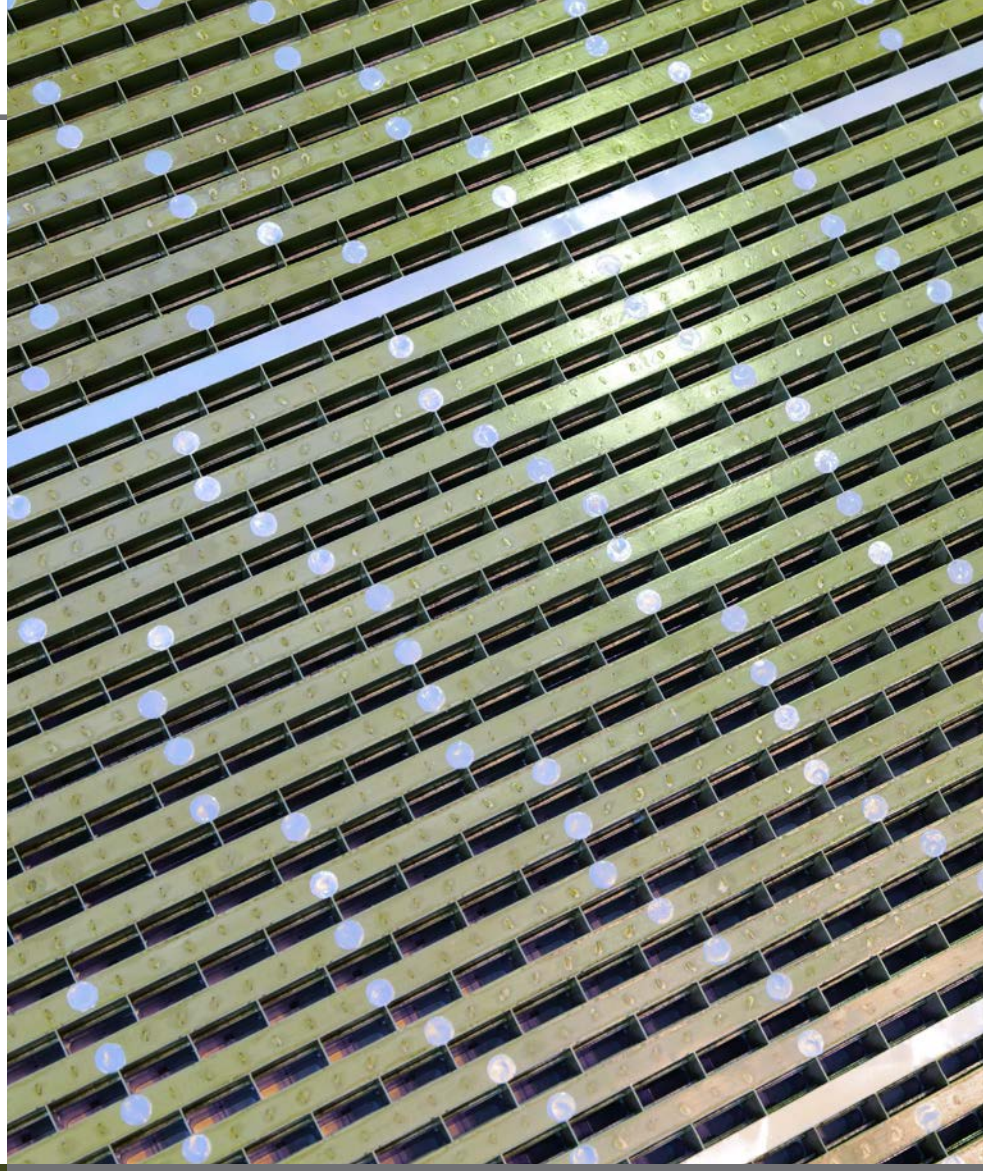


FPGA coprocessors for low-power adaptive beamforming in hybrid VPX HPEC systems

By Thierry Wastiaux

Beamforming techniques have become very important in the fields of radar, electronic warfare (EW), sonar, wireless communication, and medical imaging. These enable continuous formation of beams from array antennas (or array transducers) towards a tracked target – or a moving user in the case of wireless communication – and cancellation of all the interfering signals coming from other angles. For tactical or airborne radar and EW solutions, the execution speed of the beamforming algorithms and the low power consumption are critical. In these situations, VPX high-performance embedded computing (HPEC) hybrid field-programmable gate array (FPGA) and CPU systems appear to be the best suited approach.

The technique of adaptive beamforming has been developed for detecting and estimating the signal of interest at the output of an active electronically scanned array (AESA). Adaptive beamforming is used in radar, sonar, wireless communication systems, and medical-imaging equipment. Adaptive beamforming uses an array of antennas to achieve maximum reception in the desired direction, while signals of the same frequency from other directions are rejected. The technique computes optimal complex variables, named "weights," for measurement of the signal.

In conventional beamforming, the weights do not depend on input/output array data contrary to adaptive beamforming, aiming at suppressing noise, clutter, and jammers and maximizing signal to interference and noise ratio (SNIR). The optimum array weights need to be continuously adapted to the ever-changing environment. If the desired arrival angles change with time, the user must find a way to keep recalculating the optimum array weights. In this way, if the target is continuously moving, it can be tracked and a continuous beam can be formed towards it by using the adaptive beamforming techniques.

Adaptive beamforming principles

Let us assume an array of M antennas. The signal at each antenna $X_n(t)$ (n=1,..,M) is multiplied by complex numbers, the so-called weights W_m (m=1,..,M). The array output is then $y(t) = w^H.x(t) = \sum_{i=1,m} W_i^*.X_i(t)$ where W^* is the complex conjugate of W, and W^H is the Hermitian transpose of H.

Let us see how the array output signal can approach the desired signal d(t) that is sought in all the signals received. The difference between the array output and the desired signal is called e(t) = d(t)-y(t). If we call E[.] the statistical expectation, the Mean Square Error Criterion is $E[|e(t)|^2]$, e(t) being d(t)- $w^H.x(t)$. It can be shown that the Mean Square Error is minimum when the complex weights W_m satisfy the equation:

$W_{opt} = R^{-1}p$ where R is the correlation matrix of the input x(t), $R = E[x(t).x^H(t)]$ and p is the cross correlation vector between the input vector x(t) and the desired signal d(t) ($E(d^*(t).x(t))$. In practice to estimate the correlation matrix and the correlation vector, the samples are divided in blocks, the length of each block of samples being K. The correlation matrix and the cross correlation vector are then calculated block by block. For the correlation matrix, the K vectors of the samples of a block make a matrix MxK. This matrix is multiplied by its Hermitian transpose to build a MxM matrix R_k that is divided by the integer K. This gives an estimation of the correlation Matrix on the samples.

So getting the optimal weights (or adaptive weights) means inverting each R_k matrix and multiplying the inverse R_k^{-1} by the cross correlation vector. That is why this method of calculating the weights is called the Sample Matrix Inversion Algorithm that is suitable for rapidly changing environment.

R_k is a Hermitian square (MxM) matrix (R^H=R) that is invertible in practice, the inverse being also Hermitian. To invert the matrix several approaches are well known as the Gram-Schmidt process that can be very rapidly executed in a high-end FPGA. This process must use floating-point arithmetic to maintain the precision of the adaptive weight solution. In radar applications, the challenge is to perform this matrix inversion in a very short period of time (typically the ms) before the next pulse repetition interval of data is received. This process can be executed in CPUs or in FPGAs. It is now well established that the FPGA approach is much more performant compared to the CPU/GPU one. In its white paper WP452, Xilinx compares a Virtex-7 solution and an ARM-A9 solution and shows that the FPGA approach is consuming less energy by a factor of 18 and is cheaper by a factor of 10.

Example of a beamformer

An example of a beamformer can be built using the last generation of FPGAs and ADC coders. A Xilinx VU13P UltraScale+ FPGA offers more than 3.5 million logic

cells, 11,904 DSP enhanced slices for signal processing, and 128 times 32.75 Gb/s GTY transceivers allowing massive data flow and routing and supporting multiterabit per second throughput. The last generation of analog-to-digital (ADC) components can perform a sampling on four channels at 3 Gsps with a resolution of 14 bits. The samples are delivered to an FPGA using the JESD204B protocol, with lane speeds up to 16 Gbps and with two lanes per channel. Using only one Xilinx VU13P UltraScale+ FPGA, a beamformer can be built in the following way (for example):

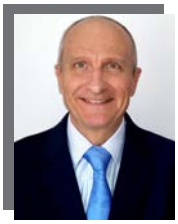
- Eight four-channel, 3 Gsps ADC sampling directly behind the array antenna
- In front of each ADC, a digital downconverter (DDC)
- Behind each DDC, a partial beamformer for the four channels, including all the principles described above with adaptive weights
- A beam adder behind all the eight partial beamformers

VPX HPEC beamforming architecture

One way to build a rugged system implementing the above approach is to use the front-end processing boards from Interface Concept as the dual Virtex-7 6U VPX board IC-FEP-VPX6b (see Figure 1) supporting two four-channel VITA 57.4 ADC FMCs or the upcoming UltraScale/UltraScale+ front-end processing boards (coming soon in the roadmap).

Figure 1 | IC-FEP-VPX6b featuring two Virtex-7 FPGAs.

Several of these boards, together with a dual Intel Broadwell processor board like the IC-INT-VPX6d/e, can make up a rugged beamformer HPEC system able to compute at a very high speed, with reduced power consumption, and using numerous continuously adapted weights to track and search the desired signals. **MES**



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