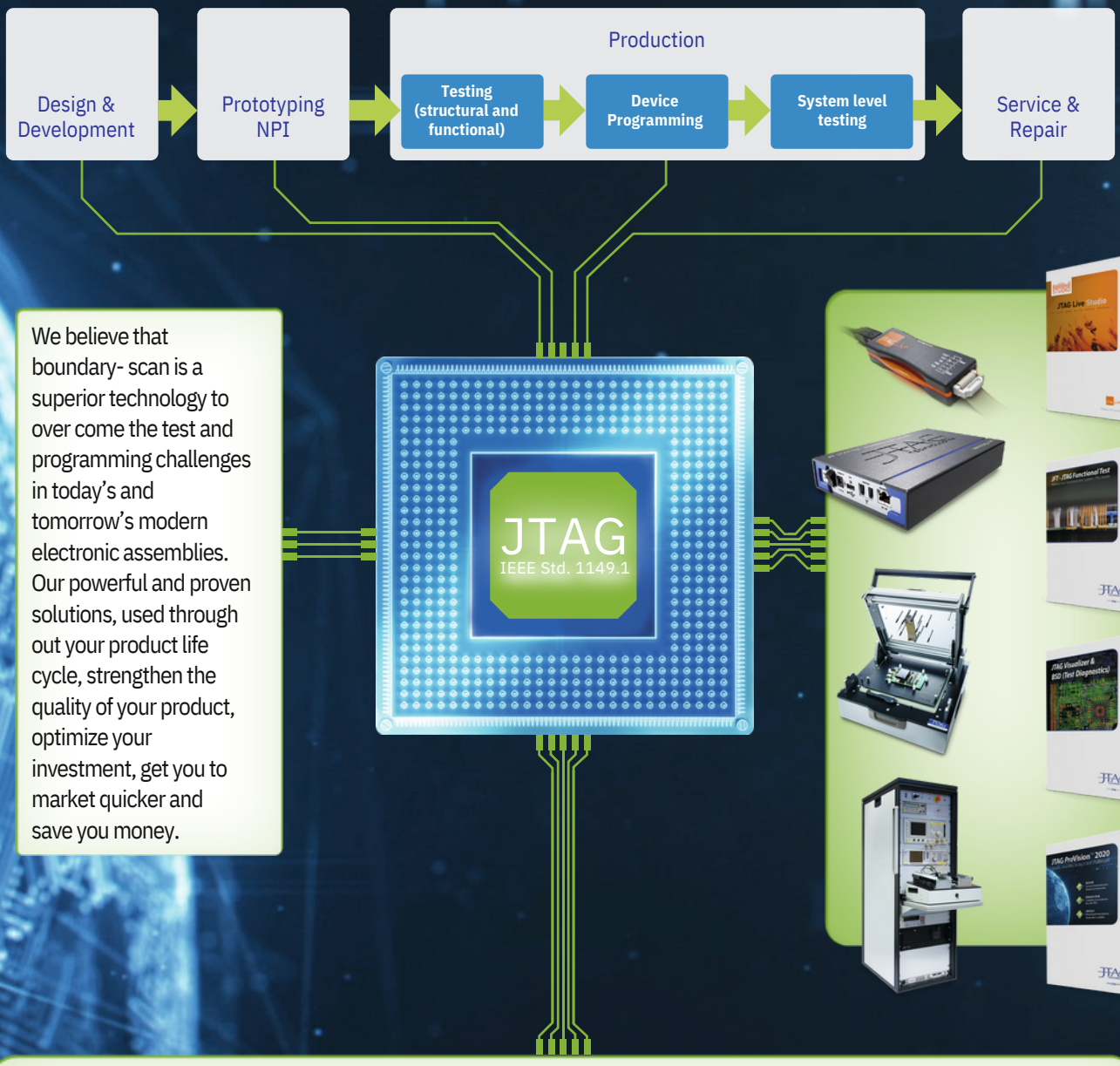
JTAG TECHNOLOGIES

Tell me about JTAG/boundary-scan!



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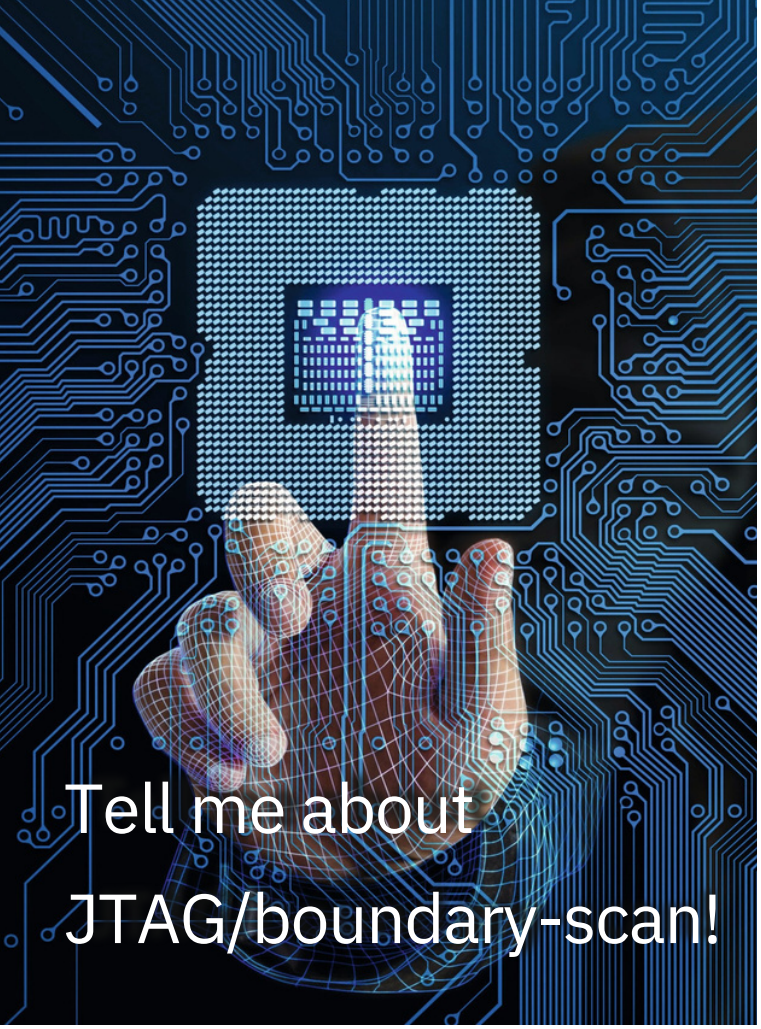

Introduction

Boundary-scan, also known as JTAG or IEEE Std. 1149.1, is a serial interface that gives access to the special embedded logic built-in into many of today's integrated circuits (ICs).

JTAG/boundary-scan provides a quick and easy method for testing electronic Printed Circuit Board Assemblies or PCBAs for manufacturing faults. It is also widely used for programming ICs such as cPLDs, FPGAs and flash memories on the circuit boards in production as well as after product manufacture if software/ firmware updates are needed.

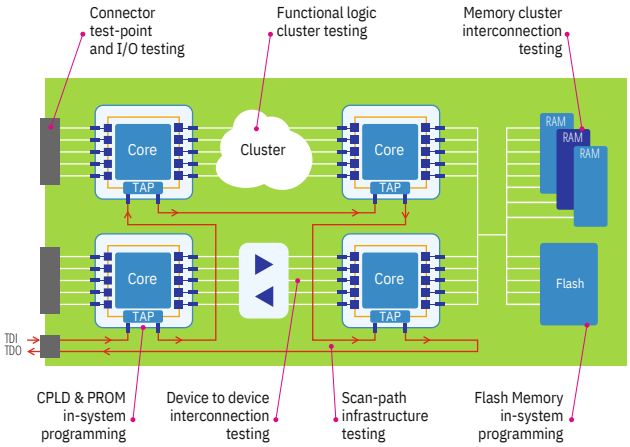

Figure 1: A PCBA with JTAG/boundary-scan

Testing Connections

What is structural testing?
Consider a connection between two devices as shown in Figure 2 where an output pin of Device A is connected to an input pin of Device B.

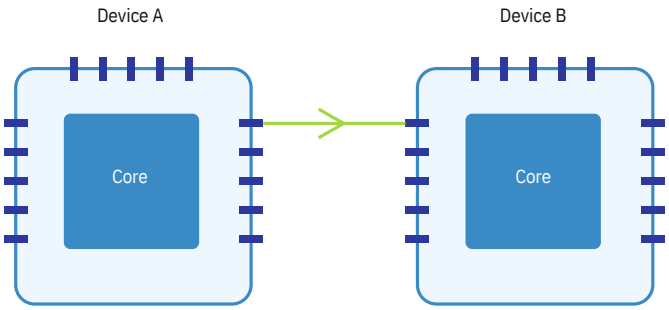

Figure 2: A connection between two devices

To verify this connection you want to drive a value on the output pin of Device A and then check if you see that value on the input pin of Device B. This way of testing is ideally done for all connections of a PCBA (Printed Circuit Board Assembly) and is called a structural test.

The big advantages of a structural test are:

1. You know exactly which connections of the PCBA are being tested and which ones are not. Therefore you know what percentage of pins / nets is tested. This percentage is called the fault coverage. A number which of course you want to get as high as possible.
2. Following the test you know immediately which connections are correct and which ones fail, thus you have immediate failure diagnostics.
3. Preparation of the test is simple since you only need to know which connections are made on the board (the netlist). The functionality of the devices is not relevant for this test.

Note that also during prototype debugging, or during repair of a board, this structural test is commonly used. Provided access to the two pins is possible this is then done by ringing out (or beeping out) the connection, traditionally by using a multimeter.

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Boundary-scan

Basic idea

Referring to Figure 2, the basic idea behind boundary-scan is that with internal cells you don't need external probing access to the pin connections you wish to test. If you can drive the output pin of Device A using a built-in drive cell, and read the result on the input pin of Device B with a built-in sense cell, you can perform the desired test, Figure 3.

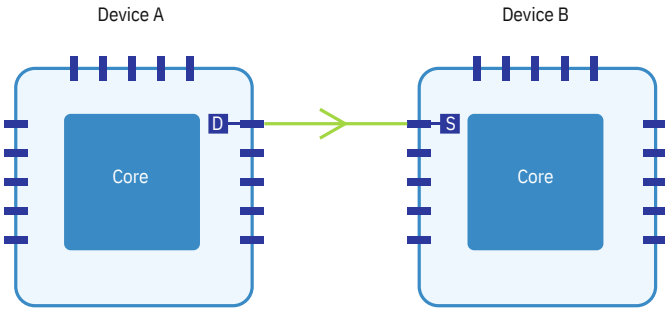

Figure 3: Adding drive and sense cells to pins for testing

These drive and sense cells should be independent of the functionality (core) of the device. This is accomplished by using a multiplexer that selects whether the pin is connected to the cell (test mode) or the core (functional mode).

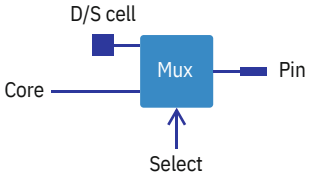

Figure 4: Multiplexer configuration; drive and sense cells independent of the functionality of the device

The cells can be built from simple logic elements like flip-flops. By adding a cell to all device pins and connecting these cells in series a shift register is created along the boundary (pins) of the chip: this is known as the boundary-scan register (BSR), figure 5.

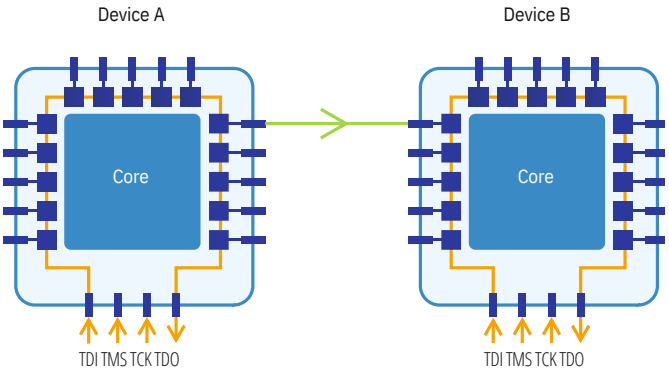

Figure 5: Shift register along the boundary (pins) of a chip

With one serial data input pin, which is called TDI (Test Data In) and one serial data output pin, called TDO (Test Data Out), we can now reach all the pins of a chip through its boundary-scan register.

A clock signal, called TCK (test ClocK), is used to shift data through the boundary-scan register while the TMS (Test Mode Select) signal controls the multiplexers at the device pins.

The signals TCK, TMS, TDI and TDO together form the test interface of the chip which is referred to as JTAG interface or TAP (Test Access Port). The boundary-scan registers of devices on a PCBA can be connected in series by connecting the TDO of one device to the TDI of the next device. TCK and TMS are connected to all devices in parallel. This results in a boundary-scan chain on the board with a single TAP for the entire chain.

Complete design

In order not to limit the use of the interface to accessing the boundary-scan register only, a mechanism was devised that allows other registers to be accessed via the TAP as well. The boundary-scan register and all these other registers are referred to as Data Registers (DR). To select between the different data registers another register, the Instruction Register (IR) is used. Also, the IR is accessed via the TDI and TDO pins of the chip.

By loading an instruction into the IR a particular DR is selected. A so-called TAP controller selects between access to the IR, or to the DR selected by the instruction in the IR. The TAP controller is a state machine with state transitions controlled by TMS. A summary of the process is as follows:

1. An instruction is loaded into the IR.
2. Data is shifted in and out of the DR selected by the instruction that was loaded into the IR.

The complete design of the JTAG/boundary-scan system is defined in the boundary-scan standard (IEEE Std. 1149.1) and a block diagram is shown in Figure 6.

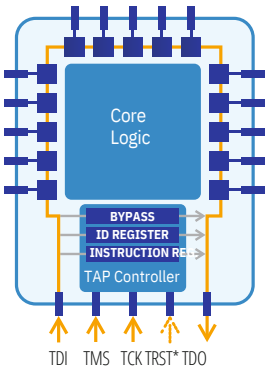

Figure 6: Boundary-scan logic in a chip

Note that a fifth optional signal, called Test ReseT (TRS) is added to the TAP interface. The active-low TRST* signal can be used to reset the TAP controller. Since this reset can also be accomplished by holding TMS high for five TCK periods, the TRST* signal is optional.*

Also in Figure 6 two other data registers are shown which have also been defined in the IEEE 1149.1 standard: these are the Bypass Register and the Device IDentification register, or ID code register.

The Bypass register can be used to shorten the total chain length and enable faster access to only those ICs and registers relevant for a particular test or action. The ID register of a device can be read to check the device type, its manufacturer and its revision level.

Figure 7 illustrates the arrangement for a number of devices on a PCBA connected in a serial scan chain.

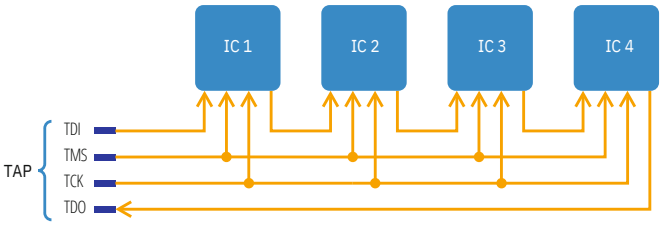

Figure 7: Boundary-scan chain on a PCBA

BSDL File

The boundary-scan logic of a device is described in a single model file known as BSDL file (Boundary-Scan Description Language), which is also part of the IEEE 1149.1 standard. For every device type, the manufacturer of that device must provide a BSDL file. Using the description in this file software tools can analyze the boundary-scan logic in a device and automatically generate tests or other boundary-scan applications, such as device programming, for a PCBA.

Applications

The boundary-scan logic on a PCBA can be used for testing connections. Not only direct connections between boundary-scan devices, but also connections through transparent devices such as series resistors and buffers for example, as well as connections through logic gates. The presence of pull-up and pull-down resistors and connections to memory devices and micro processor peripherals can also be tested.

But it's not only testing that is possible with JTAG/boundary-scan. Also program ming of devices such as cPLDs and FPGAs as well as flash memories is done via the JTAG interface. Software debugging is another application which uses the JTAG interface. In most of today's microcontrollers and DSPs the debug logic for software debugging is accessed and controlled through the TAP.

Additional standards

IEEE Std. 1149.1, initially ratified in 1990, defines the TAP and covers the digital I/O pins of a device. After this first standard additional standards were developed to define the logic for other types of I/O pins. IEEE Std. 1149.4 defines the logic for analog device pins. IEEE Std. 1149.6 defines the logic for capacitor-coupled high speed I/O pins. These three standards are sometimes also briefly referred to as Dot 1, Dot 4 and Dot 6 respectively. The TAP as defined in Dot 1 is also used as interface to access the logic defined in Dot 4 and Dot 6. Other standards which define logic that can be accessed through the TAP interface of Dot 1 have also been defined, for example 1532 for programming cPLDs and FPGAs and 1687 for accessing embedded instruments.

The JTAG interface in Microcontrollers and DSPs

A significant number of microprocessors and DSPs include a JTAG port for software debugging, however, some don't actually have a boundary-scan register. With these devices the micro - processor debug logic can now be used to perform 'JTAG' testing and other applications such as flash memory programming. The debug logic is then used to set-up and control embedded peripherals and leverage those elements to test connections with the outside world – typically these peripherals will include memory controllers, ADCs and DACs, control and communi-cation interfaces such as PWMs and PHYs.

Hardware and Software

Hardware and software is needed to control the boundary-scan logic and drive data through the TAP and the registers in the chains. Special, advanced software can automati-cally generate JTAG/boundary-scan applications from CAD data and device models.

A broad range of hardware and software tools is available with different capabilities and performance. This gives you the possibility to configure the boundary-scan solution that optimally fits the needs of your application area. For example tools for hardware debugging during prototype bring-up, testing and device programming in production, or repair and device re-programming for product upgrades in service.

The hardware and software tools are the subject of two other papers in this "Tell me about" series: Tell me about JTAG hardware and Tell me about JTAG Software.

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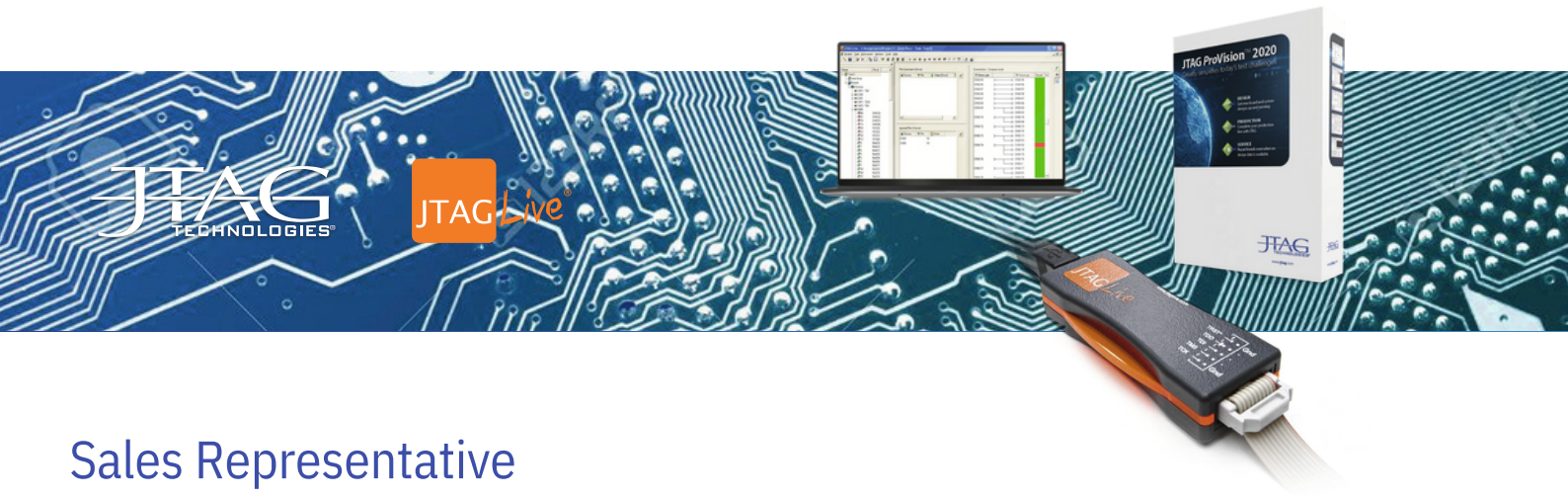

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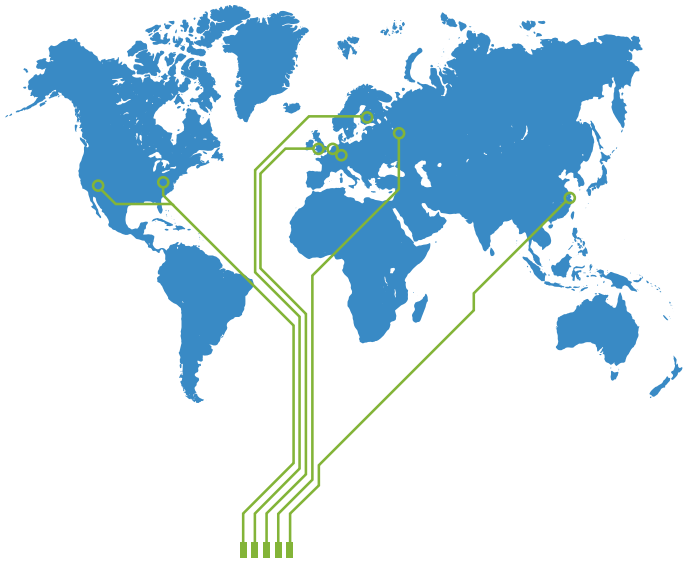

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